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EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,502	ERTLE ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19,22-39 and 41* is/are pending in the application.

4a) Of the above claim(s) *34-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,22-33,38,39,41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 27, 2009 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18, 19, 22 - 33, 38, 39, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In particular, independent claims 18, 28, 38, and 39 recite the limitation "*the passive first region having no components of an integrated circuit*", however it is unclear and ambiguous what is meant by a component of an integrated circuit. For example, figure **2** of the current application shows that the designated passive region **5** comprises both interconnect vias **9**, a n-doped well **25**, and dielectric layers **8** and **11**, all of which may be considered to be components of an integrated circuit since these components are well-known in the art to be used in integrated circuits. However, figure 2 also shows

active region **7** comprising an active component **(**MOS transistor) **24**, which is not within the passive region **5**. Therefore, a best-deemed interpretation is made, and the limitation "*the passive first region having no components of an integrated circuit*" is interpreted as "*the passive first region having no active components*." Claims 19, 22 – 27, and 41 depend from claim 18, and claims 29 – 33 depend from claim 28.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 18, 26, 27, 38, 39 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 6,159,826).

a. Regarding claim 18, **Kim discloses semiconductor chip** (e.g. figures 4 and 5) **comprising:**

a passive first region on a top side of the semiconductor chip (region 34);

an active second region on the top side of the semiconductor chip (region 32);

an arrangement of contact areas (contact areas 56b) **and test areas** (test areas 56a) **having respective top surfaces which are arranged in a common plane** (e.g. as seen in figure 5, the dope surfaces of the contact and

test areas are in a common plane) **and exposed to the top side of the semiconductor chip through contact windows and test windows** (windows formed by the absence of layer 57 on the substrate**), respectively, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in the passive first region** (contact areas 56b are in the passive region 34), **the passive first region having no components of an integrated circuit** (as seen in figure 5, there are no active devices in this region. Please refer to the USC 112, 2nd paragraph rejection above), **the test areas being arranged in the active second region** (test areas 56a are in the active region 32), **the active second region having components of an integrated circuit** (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit)**; and**

an insulating layer (insulating layer 53, disclosed in col. 3, line 33) **having through contacts** (through contacts 55) **arranged in the region of the conduction web and extending from the conduction web to a lower plane** (as seen in figure 5)**, the through contacts being connected to interconnects** (interconnects 52a and 52) **that are connected to electrodes of the components of the integrated circuit** (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 5, the top surfaces of the contact and test areas are free from the through contacts).

b. Regarding claim 26, **Kim discloses the semiconductor chip of claim 18, as cited above, comprising wherein the conduction web is formed in T** (e.g. as seen in figure 4, a T is formed from the conduction web 36 at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to the width of the contact areas** (e.g. as seen in figure 5, the transverse bar of the T has a vertical width of equal to the vertical width of the contact area 56b) **and having through contacts to interconnects** (through contacts 55 to interconnects 52), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (the claim limitation of "*a width determined in response to the maximum current loading*" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction web is capable of supplying current during testing, therefore the structure anticipates the claimed limitation).

c. Regarding claim 27, **Kim discloses the semiconductor chip of claim 18, comprising wherein the test areas have a width (b_p) about equal to a**

width of the contact areas and have a length (l_p) greater than their width (b_p) (e.g. as seen in figure 5, the vertical width of the test areas 56a and contact areas 56b are about equal, and the horizontal length of the test areas are greater than the their vertical width).

d. Regarding claim 38, **Kim discloses a semiconductor wafer** (e.g. figures 3 - 5, wafer 30) **comprising:**

a plurality of semiconductor chips (chips 32) **having a passive first region (first region 34) and an active second region** (second region 32), **the semiconductor chips having an arrangement of contact areas** (contact areas 56b) and test areas (test areas 56a) **which are arranged in a common plane** (e.g. top surface of the areas are in a common plane) **and are electrically conductively connected to one another via a conduction web that lies in the common plane** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b);

the contact areas being arranged in the passive first region of the top side of the semiconductor chip (contact areas 56b are in the passive region 34)**, the passive first region having no components of an integrated circuit** (as seen in figure 5, there are no active devices in this region. Please refer to the USC 112, 2nd paragraph rejection above); **and**

the test areas being arranged in the active second region of the top side of the semiconductor chip (test areas 56a are in the active region 32), **the**

active second region having components of an integrated circuit (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit); **and**

an insulating layer (insulating layer 53, disclosed in col. 3, line 33) **having through contacts** (through contacts 55) **arranged in the region of the conduction web and extending from the conduction web to a lower plane** (as seen in figure 5), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 5, the top surfaces of the contact and test areas are free from the through contacts).

e. Regarding claim 39, **Kim discloses a semiconductor chip** (e.g. figures 4 and 5, chip 32) **comprising:**

a passive first region on a side of the semiconductor chip (region 34);

an active second region on the side of the semiconductor chip (region 32);

an arrangement of contact areas (contact areas 56b) **and test areas** (test areas 56a) **which are arranged in a common plane** (e.g. as seen in figure 5, the dope surfaces of the contact and test areas are in a common plane) **and**

are in each case electrically conductively connected to one another via a conduction web that lies in the common plane (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in the passive first region** (contact areas 56b are in the passive region 34), **the passive first region having no components of an integrated circuit** (as seen in figure 5, there are no active devices in this region. Please refer to the USC 112, 2nd paragraph rejection above), **the test areas being arranged in the active second region** (test areas 56a are in the active region 32), **the active second region having components of an integrated circuit** (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit); **and**

an insulating layer (insulating layer 53, disclosed in col. 3, line 33) **having through contacts** (through contacts 55) **arranged in the region of the conduction web and extending from the conduction web to a lower plane** (as seen in figure 5), **the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit** (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 5, the top surfaces of the contact and test areas are free from the through contacts).

f. Regarding claim 41, **Kim discloses the semiconductor chip of claim 18, wherein each of the contact areas is electrically conductively connected to a respective one of the test areas by the conduction web extending between and in the same plane as the contact area and the respective test area** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim.

g. Regarding claim 28, **Kim discloses an electronic device** (e.g. figures 4 and 5) **comprising:**

a semiconductor chip (semiconductor chips 32, disclosed in col. 3, line 8), **the semiconductor chip having an arrangement of contact areas** (contact areas 56b) **and test areas** (test areas 56a) **which are arranged in a common plane** (e.g. as seen in figure 5, the dope surfaces of the contact and test areas are in a common plane) **and are in each case electrically conductively connected to one another via a conduction web that lies in the common**

plane (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in a passive, first region of the top side of the semiconductor chip** (passive region 34), **the passive first region having no components of an integrated circuit** (as seen in figure 5, there are no active devices in this region. Please refer to the USC 112, 2nd paragraph rejection above);

the test areas being arranged in an active, second region of the top side of the semiconductor chip (active region 32), **the active second region having components of an integrated circuit** (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit);

the test areas and contact areas being formed in the same interconnect plane (e.g. as seen in figure 5); **and**

the length (l_p) of the test areas being greater than the width (b_p) thereof (e.g. as seen in figure 5, the vertical length of the test area is greater than the horizontal width); **and**

an insulating layer (insulating layer 53, disclosed in col. 3, line 33) **having through contacts** (through contacts 55) arranged in the region of the conduction web and extending from the conduction web to a lower plane (as seen in figure 5), **the through contacts being connected to interconnects** (interconnects 52a and 52) **that are connected to electrodes of the**

components of the integrated circuit (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 5, the top surfaces of the contact and test areas are free from the through contacts).

Kim is silent with respect to explicitly stating that the length (l_p) of the test areas being at least approximately 1.5 times greater than the width (b_p) thereof. However, as seen in figures 6 and 16, the vertical length of the test areas are at least greater than their horizontal width. Although the figures are not indicated to be drawn to scale, it would have been obvious for one of ordinary skill in the art at the time the invention was made to make the structure of Kim such a that the horizontal length of the test areas are at least approximately 1.5 times greater than their vertical width, since often the thickness (vertical width) of the layers are much thinner than the (horizontal) length of the layers, and the figures imply such a configuration for the device. Furthermore it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make such a modification in order to accommodate a large test probe while having a thin layer in order to minimize device thickness.

8. Claims 19, 22 – 25, and 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Henson (US 6,133,054, prior art of record).

a. Regarding claims 19 and 29, **Kim discloses the device of claims 18 and 28, as cited above, respectively, wherein the insulating layer** (figure 5, layer 53) **is arrange between the components of an integrated circuit** (e.g. N+ and P+ regions in substrate 51) **and the test areas of the semiconductor chip** (test areas 56a). **Kim is silent with respect to disclosing the insulating layer includes silicon dioxide and/or silicon nitride.**

Henson discloses that insulating layers in semiconductor devices may including silicon dioxide or silicon nitride (col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim such that the insulating layers including silicon dioxide and/or silicon nitride since Kim simply discloses the layers to be insulating, and it was well-known in the art that insulating layers used in semiconductor devices may be formed from silicon oxide or silicon nitride, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide and/or silicon nitride as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

b. Regarding claim 22, **Kim discloses the semiconductor chip of claim 18, as cited above, but is silent with respect to the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.**

Henson discloses that interconnects to electrodes of components of an integrated circuit may comprise copper (e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use copper for the material of the interconnect structure of Kim since it was well-known in the art that copper can be used for interconnects in test circuits for integrated circuits, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use copper as an interconnect structure since is a low-resistance conductor that is relatively inexpensive.

c. Regarding claim 23, **Kim discloses the semiconductor chip of claim18, as cited above, comprising wherein the contact areas and the test areas at**

their edges and the conduction web on its top side have a insulation and passivation layer (layer 57, disclosed col. 3, line 44). **Kim is silent with respect to disclosing the insulating and passivation layer is a multilayer structure.**

Henson discloses that insulation and passivation layers on semiconductor devices may be formed as a multilayer structure (e.g. figure 7, layers 722 and 724, disclosed in col. 4, lines 30 - 32).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the structure of Kim such that the top insulation and passivation layer comprises multiple layers since Henson discloses a similar device with multiple insulating and passivation layers form atop the device. One would have been motivated to form a multilayer insulation and passivation layer in order to form a multilayer protection layer that is resistant to physical stress, moisture (as discussed in Henson, col. 4, line 30), and is thermally stable.

d. Regarding claim 24, **Kim in view of Henson disclose the semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web** (e.g. layer 57 of Kim, or layers 722 and 724 of Henson).

Both Kim and Henson are silent with respect to the layer being silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim in view of Henson such that the insulating layer on the top of the device includes silicon dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

e. Regarding claim 25, **Kim in view of Henson the semiconductor chip of claim 23, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 - 32).

f. Regarding claim 30, **Kim in view of Henson disclose the electronic device of claim 29, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper**

alloy (Henson: e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 – 23).

g. Regarding claim 31, **Kim in view of Henson disclose the electronic device of claim 30, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer** (e.g. figure 5 of Kim shows insulation and passivation layer 57, and figure 7 of Henson shows a multilayer insulation and passivation layer, including layers 722 and 724, disclosed in col. 4, lines 30 – 32).

Both Kim and Henson are silent with respect to the multilayer insulation and passivation layer including silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim in view of Henson such that the insulating layer on the top of the device includes silicon dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been

motivated to use silicon dioxide as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

h. Regarding claim 32, **Kim in view of Henson disclose the electronic device of claim 30, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 – 32).

i. Regarding claim 33, **Kim in view of Henson disclose the semiconductor chip of claim 29, as cited above, comprising wherein the conduction web is formed in T** (Kim: e.g. as seen in figure 4, a T is formed from the conduction web 36 at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas** (Kim: e.g. as seen in figure 5, the transverse bar of the T has a vertical width of equal to the vertical width of the contact area 56b) **and having through contacts to interconnects** (Kim: through contacts 55 to interconnects 52), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (the claim limitation of "*a width determined in response to the maximum current loading*" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction

web is capable of supplying current during testing, therefore the structure of Kim in view of Henson anticipates the claimed limitation).

Response to Arguments

9. Applicant's arguments with respect to claims 18, 28, 38, and 39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
March 31, 2009